REMARKS

Claims 1-7 were pending of which Claims 1-7 were rejected. Claim 1 has been amended. The amendments can be fully supported by the specification and figures of the present invention as originally filed. Therefore, there is no new matter added therein. In view of the foregoing amendments and the following remarks, reconsideration of the present patent application is respectfully requested.

Drawings

Applicant notes that in the drawings are objected to in the Office Action Summary, but no objection is provided in the Detailed Action. Applicant respectfully requests that the Office Action Summary is updated to reflect that the drawings are accepted or that the Examiner provide a explanation of the objection.

Claim Rejections – 35 U.S.C. §103

Claims 1-7 were rejected under 35 U.S.C. §103(a) as being unpatentable over US Patent No. 5,854,792 issued to Konishi et al ("Konishi") in view of US Patent No. 6,108,345 issued to Zhang ("Zhang") in further view of US Patent No. 6,658,015 issued to Merchant et al. ("Merchant"). Reconsideration is respectfully requested.

Amended Claim 1 recites "**a gateway apparatus** for using in performing communication between wide area networks (WAN) to local area networks (LAN)" that includes "a plurality of input/output ports", "a shared buffer device", "a plurality of medium access control units", "a memory device", and "a central processing unit". The Examiner considers that Konishi has disclosed a network connection apparatus 2 including a plurality of input/output ports for connecting the two networks, a buffer device for accessing packets, and a memory device for storing the packets. It should be clarified, however, that the LAN switch circuit 13 of the network connection apparatus 2 (corresponding to the gateway apparatus of Claim 1) disclosed in Konishi, which is interposed between each LAN 1a-1n and a corresponding LAN control section 8a-8n, includes **a plurality of data receiving buffers 17a-17n** dedicated to the LANs 1a-1n, respectively, while the gateway apparatus of Claim 1 has a single "**shared buffer device** connected to the plurality of input/output ports". Furthermore, it is clear from the descriptions and the illustration of Fig. 6 of Konishi that the memory device disclosed therein is not electrically connected to the buffer device, while the gateway of the present

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invention is characterized in that **the memory device is electrically connected to the shared buffer device** for storing the packets sent from the buffer device, as recited in Claim 1.

Moreover, the Examiner correctly notes that Konishi does **not** disclose "**a plurality of medium access control units** corresponding to said input/output ports and electrically connected between said shared buffer device and said input/output ports for performing an accessing operation between said shared buffer device and said input/output ports", and does **not** disclose "**a central processing unit** electrically connected to said memory device and said medium access control units for processing said packets stored in said memory device, and organizing said medium access control units to change said input/output ports according to a required transporting path , thereby performing said communication between said LAN and said WAN". The Examiner relies on Merchant as disclosing medium access control units 20 and the central processing unit 32. Applicant maintains that one skilled in the art at the time of the invention would not have modified the ports within the network connection apparatus as disclosed in Konishi, with connection of a medium access control (MAC) module and the central processing unit (CPU) recited in Merchant to achieve the features of gateway apparatus of the present invention. The detailed reasons are provided as follows.

Merchant discloses that the multiport switch 12 only includes interfaces for the memory and the CPU and does **not** include the actual memory and CPU themselves, as is recited in Claim 1. For example, Fig. 2 of Merchant clearly shows that only the memory interface 44 and the CPU interface 50 are included in the multiport switch 12 (corresponding to the gateway apparatus of Claim 1). Fig. 1 of Merchant clearly shows that the memory device 36 itself and the host CPU 32 itself are **not** disposed within the multiport switch 12. Thus, Merchant discloses that the memory device 36 and the host CPU 32 are only connected to the memory interface 44 and the CPU interface 50 within the multiport switch 12. Claim 1, on the other hand, specifically recites **that the CPU and the memory device are within the gateway apparatus** and that the CPU is "electrically connected to said memory device and said medium access control units for processing said packets stored in said memory device, and organizing said medium access control units to change said input/output ports according to a required transporting path , thereby performing said communication between said LAN and said WAN." Thus, Merchant lacks the disposition and connection features of the CPU in comparison with Claim 1. Merchant requires the use of external components to operate with its network switch, which requires more complicated conformations and circuit designs over

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the gateway apparatus of Claim 1. Accordingly, the advantage of compact and simpler design of the gateway apparatus of Claim 1 is incapable of being achieved by the cited references. Accordingly, Merchant fails to make up for the deficiencies of Konishi or even Konishi combined with Zhang.

Additionally, Applicant maintains that the Examiner's motivation to modify Konishi with Merchant, e.g., to be able to receive and transmit data frames to the appropriate destination, higher throughput, and allow multiple frames to be processed simultaneously, is based on impermissible hindsight. The Examiner simply relies on benefits of Merchant but fails to provide a reason why one of ordinary skill in the art would combine Merchant with Konishi. Because all patents must have some utility (35 U.S.C. §§101, 112), it is inappropriate to merely cite one patent's (Merchant) benefit as the sole reason to modify another patent (Konishi), as the Examiner has done here.

To sum up, the gateway apparatus recited in Claim 1 of the present application not only has the distinct structural features over the cited reference, but there is no reason (other than hindsight) to combine the cited references as suggested. Therefore, withdrawal of the rejection is respectfully requested. Furthermore, since the independent Claim 1 is patentable over the cited references, the dependent Claims 2-6 are also patentable, for at least the same reasons, owing to their dependency from the patentable Claim 1.

Claims 1-7 remain pending, of which Claim 1 was amended. For the above reasons, Applicants respectfully request allowance of Claims 1-7. Should the Examiner have any questions concerning this response, the Examiner is invited to call the undersigned at (408) 982-8202.

CERTIFICATE OF FACSIMILE TRANSMISSION

I hereby certify that this correspondence is being facsimile transmitted to the U.S. Patent and Trademark Office to the fax number 571-273-8300 on June 28, 2006.

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